REMARKS

The claims are claims 1 to 11.

The application has been amended at many locations to correct minor errors and to present uniform language throughout. The amendments include correction of a double use of reference numbers 204 and 205 in Figure 2.

The drawings have been amended to correct a double use of reference numbers 204 and 204 in Figure 2.

Claims 1, 4 and 6 are amended. New claims 8 to 11 are added. Claims 1, 4 and 6 are amended in response to the rejection under 35 U.S.C. 112. These amendments do not change the scope of these claims. New claims 8 to 11 correspond to claims 1 to 4 except they recite various pipeline stages when event occur.

Claims 1 to 4 and 6 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Amended claim 1 no longer presents an ambiguity as to whether the remote queue counter or the data source is connected to the data destination. Claim 1 has been amended to make clear that it is the remote queue counter that is connected to the data destination.

Claim 4 has been amended to change the limitation "said master queue" to "said master queue counter." The antecedent basis for the master queue counter is found in claim 1.

Claim 6 has been amended to change the limitation "remote queue counter" to "remote count." The antecedent basis for the remote count is found in claim 5.

Claims 1 to 7 were rejected under 35 U.S.C. 102(e) as anticipated by Dennin et al U.S. Patent No. 6,401,149. The summary of this rejection at page 2, lines 12 and 13 only mention claims 1

to 4. However, the text of the OFFICE ACTION at page 5, line 12 to page 6, line 14 applies the rejection to claims 5 to 7.

Claims 1 and 5 recite subject matter not anticipated by Dennin et al. Claim 1 recites "a master queue counter storing a master count indicative of a number of data entries available for data storage within said first-in-first-out buffer memory" and "decrement said master count upon allocation of data at said data source to be stored in said first-in-first-out buffer memory." Claim 5 recites "maintaining a master count indicative of a number of data entries available for data storage within a first-in-first-out buffer memory" and "decrementing the master count upon allocation of data at the data source to be stored in the first-in-first-out buffer memory." The OFFICE ACTION cites FIFO utilization counter 414 illustrated in Figure 4 and column 8, line 57 to 61 of Dennin et al as anticipating both the master queue counter/master and the remote queue counter/remote count. Dennin et al states at column 8, lines 57 to 65:

> "For example, the FIFO utilization counter 414 may track the amount of FIFO memory locations utilized, and hence, the number of FIFO locations which are not being utilized. In one embodiment, the utilization counter 414 may be read or written to as register by the local microprocessor 108 and/or microcontroller 120. The readable count provides the number of bytes stored in the FIFO array 402."

This portion of Dennin et al states that the "readable count" stored in FIFO utilization counter 414 is "the number of bytes stored in the FIFO array 402." This corresponds to the remote queue counter recited in claim 1 and the remote count recited in claim 5. At best this teaching indicates that FIFO utilization counter 414 anticipates one of the master queue counter/master count and remote queue counter/remote count. This teaching of Dennin et al clearly implies that the other quantity must be

inferred from the contents of FIFO utilization counter 414. The Applicant respectfully submits that Dennin et al elsewhere discloses that FIFO utilization counter 414 stores the number of entries in the FIFO storing data. Dennin et al states at column 9, lines 58 to 60 states:

> "A pause signal is generated when a write operation to the access register 416 is attempted when the utilization counter count equals the FIFO size. This ensures that FIFO data is not overwritten."

The "utilization counter count" is a reference to FIFO utilization counter 414. Pausing a write operation "when the utilization counter count equals the FIFO size" to avoid overwriting, implies FIFO utilization counter 414 stores the number of FIFO entries currently storing data. Dennin et al states at column 10, lines 11 to 13:

> "The utilization word count is decremented each time a read operation is performed. The pause signal is generated if a read operation from the FIFO access register is attempted when the FIFO utilization count is zero."

Both "utilization word count" and "FIFO utilization count" refer to FIFO utilization counter 414. Decrementing on a read from the FIFO and pausing reads when the count is zero implies FIFO utilization counter 414 stores the number of FIFO entries currently storing data. Dennin et al states at column 10, lines 17 to 21:

> "The memory locations may loaded by the performance of a write operation from the access register, which would thereby increment the utilization count."

The "utilization count" refers to FIFO utilization counter 414. Incrementing this utilization count upon a write to the FIFO implies FIFO utilization counter 414 stores the number of FIFO

entries currently storing data. These recitations of Dennin et al correspond to the claimed remote queue counter in claim 1 and the remote count in claim 5. Thus Dennin et al fails to anticipate the master queue counter recited in claim 1 nor the master count recited in claim 5.

Dennin et al discloses only a single counter where claims 1 and 5 require two. It is possible as a theoretical matter for a single reference structure to anticipate two claimed structures. However, in this instance the Applicant submits that the two claimed limitations cannot be anticipated by a single FIFO utilization counter 414. Claims 1 and 5 recite different data is stored. Claims 1 and 5 recite "a master count indicative of a number of data entries available for data storage within said first-in-first-out buffer memory" and "a remote count indicative of a number of data entries within said first-in-first-out buffer memory currently storing data." It is impossible for the single FIFO utilization counter 414 to store these different claimed amounts. Claims 1 and 5 recite different changes to the two counts on occurrence of the same event. Upon allocation of data to be stored in the first-in-first-out buffer memory, claim 1 recites "to decrement said master count" and "incrementing said remote count." Upon allocation of data to be stored in the first-in-first-out buffer memory, claim 5 recites "decrementing the master count" and "incrementing the remote count." On transfer of data out of the first-in-first-out buffer memory, claim 1 recites "decrementing said remote count and generating a decrement confirmation signal" and "incrementing said master count upon receipt of said decrement confirmation signal." On transfer of data out of the first-in-first-out buffer memory, claim 5 recites "decrementing said remote count" and "incrementing said master count upon confirmation of decrementing the remote count." The single FIFO utilization counter 414 of Dennin et al cannot anticipate these opposite responses to

the same event. This language clearly requires two counters in claim 1 and two counts in claim 5. Two counters/counts are required because the above quoted portions of the claims recite opposite results (increment/decrement) on the counters/counts in response to the same events. The single FIFO utilization counter 414 cannot both increment and decrement in response to allocation of data to the FIFO. Accordingly, claims 1 and 5 are allowable over Dennin et al.

Claims 2 and 6 recite subject matter not anticipated by Dennin et al. Claim 2 recites "said master queue counter is initialized to said predetermined number of data entries of said first-in-first-out buffer memory; and said remote queue counter is initialized at zero." Claim 6 recites "initializing the master count to the number of data entries of the first-in-first-out buffer memory; and initializing the remote count to zero." The OFFICE ACTION cites Dennin et al at column 8, lines 42 to 56 as anticipating this subject matter. In fact, this portion of Dennin et al includes no mention of FIFO utilization counter 414 or any related term, which the OFFICE ACTION states anticipates the master queue counter/master count and the remote queue counter/remote count. Thus this portion of Dennin et al cannot anticipate any initialization of either counter recited in claim 2 or count recited in claim 6. Dennin et al states at column 16, lines 1 to 4:

> "The write pointer (WP) 410, read pointer (RP) 412, transfer counter 406, and word count, based on the utilization counter 414, are automatically initialized with default values."

This disclosure mentions FIFO utilization counter 414 and initialization but fails to state what is the default value. Dennin et al states at column 16, lines 37 to 39:

"The write pointer (WP) 410, read pointer (RP) 412, transfer counter 406, and utilization counter 414 are automatically initialized to default values."

This likewise mentions FIFO utilization counter 414 and initialization but fails to state what is the default value. Thus Dennin et al does not anticipate the initialization of the master queue counter (claim 2) or the master count (claim 6) to the number of entries in the first-in-first-out buffer memory. Dennin et al fails to disclose the remote queue counter recited in claim 2 nor the remote count recited in claim 6. Therefore Dennin et al cannot anticipate initialization to zero as recited in claims 2 and 6. The OFFICE ACTION presents arguments regarding initialization of the remote queue counter but points to no part of Dennin et al supporting these arguments. Accordingly, claims 2 and 6 are allowable over Dennin et al.

Claims 3 recites subject matter and claim 5 recites additional subject matter not anticipated by Dennin et al. Claim 3 recites "said data source may allocate data to said first-in-first-out buffer memory only if said master queue counter indicates a non-zero number of data entries available for data storage within said first-in-first-out buffer memory." Claim 5 recites "allocating data from the data source to the first-in-first-out buffer memory only when the master count is non-zero." The OFFICE ACTION cites Dennin et al at column 13, lines 12 to 26 as anticipating this subject. The Applicant respectfully submits that this portion of Dennin et al fails to mention FIFO utilization counter 414 or any other related term, which the OFFICE ACTION states anticipates the claimed mater queue counter/master count. Since both claims 3 and 5 recite allocation of data to the first-in-first-out buffer memory dependent upon the master count, this portion of Dennin et al fails to anticipate this subject matter. Accordingly, claims 3 and 5 are allowable over Dennin et al.

Claims 3 recites additional subject matter and claim 5 recites further subject matter not anticipated by Dennin et al. Claim 3 recites "said data destination reads said first-in-first-out buffer memory only if said remote queue counter is non-zero." Claim 5 recites "transferring data from the first-in-first-out buffer memory to the data destination only if the remote count is non-zero." The OFFICE ACTION cites column 12, lines 25 to 47 as anticipating this subject matter. The Applicant respectfully submits that this portion of Dennin et al fails to mention FIFO utilization counter 414 or any other related term, which the OFFICE ACTION states anticipated the remote queue counter/remote count. Since both claims 3 and 5 recite read of data out of the first-in-first-out buffer memory dependent upon the remote count, this portion of Dennin et al fails to anticipate this subject matter. Accordingly, claims 3 and 5 are allowable over Dennin et al.

Claims 4 and 7 recite subject matter not anticipated by Dennin et al. Claim 4 recites "said data source may selectively annul allocation of data of said data source to be stored in said first-in-first-out buffer memory." Claim 7 recites "selectively annulling allocation of data of the data source to be stored in the first-in-first-out buffer memory." The OFFICE ACTION cites special commands taught in columns 11 and 12 of Dennin et al as anticipating this subject matter. This commands listed in Table 2 at the top of column 12 include: Clear FIFO; Stop FIFO; Load FIFO; Unload FIFO; Load FIFO with BCRC check; Unload FIFO with BCRC Generation; Read from Buffer Memory; Write to Buffer Memory; Fetch FCP Command; and Update Current FCP Command pointer. The Applicant respectfully submits that none of these commands consists of selectively annulling allocation of data of the data source to be stored in the first-in-first-out buffer memory. The OFFICE ACTION includes no arguments why any of these commands anticipates the

claimed selectively annulling allocation. Accordingly, claims 4 and 7 are allowable over Dennin et al.

Claims 4 and 7 further recite subject matter not anticipated by Dennin et al. Claim 4 recites "said master queue counter is further connected to said data source to increment said master count upon receipt of said annul increment signal.." Claim 7 recites "incrementing the master count upon annulling allocation of data." The OFFICE ACTION cites special commands taught in columns 11 and 12 of Dennin et al as anticipating this subject matter. The Applicant respectfully submits that the portions of Dennin et al cited in the rejection fail to mention FIFO utilization counter 414 or any related term, which the OFFICE ACTION states anticipates the master queue counter/master count. Thus this portion of Dennin et al cannot anticipate change to the recited count. Accordingly, claims 4 and 7 are allowable over Dennin et al.

New claims 8 to 11 recite subject matter not anticipated by Dennin et al. New claims 8 to 11 correspond to claims 1 to 4 except they recite various pipeline stages when event occur. Dennin et al includes no mention of the various pipeline stages recited in claims 8 to 11. Accordingly, claims 8 to 11 are allowable over Dennin et al.

The Applicant respectfully submits that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicant request that the Examiner contact Applicant's attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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